IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 13782US03

In the Application of:

Elzur, et al.

Serial No.: 10/652,267

Filed: August 29, 2003

For: SYSTEM AND METHOD FOR TCP OFFLOAD

Art Unit: 2143

Examiner: Avellino, Joseph E.

Confirmation No. 1986

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from an Office Action dated October 7, 2005 ("the Final Office Action"), in which claims 1-33 were finally rejected. The Applicants respectfully request that the Board of Patent Appeals and Interferences reverse the final rejection of claims 1-33 of the present application. The Applicants note that this Appeal Brief is timely filed within the period for reply that ends on May 24, 2006, pursuant to the Notice of Panel Decision from Pre-Appeal Brief Review dated April 24, 2006.

REAL PARTY IN INTEREST
(37 C.F.R. § 41.37(c)(1)(i))

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 013562, Frame 0360 in the PTO Assignment Search room.

RELATED APPEALS AND INTERFERENCES
(37 C.F.R. § 41.37(c)(1)(ii))

Not applicable.

STATUS OF THE CLAIMS
(37 C.F.R. § 41.37(c)(1)(iii))

Claims 1-33 were finally rejected. Pending claims 1-33 are the subject of this appeal.

The present application includes claims 1-33, which are pending in the present application.[1] Claims 1-5, and 7-33 remain rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,757,746 ("Boucher").[2] Claim 6 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher.[3] The Applicants identify claims 1-33 as the claims that are being appealed. The text of the pending

[1] *See* Present Application ("Application") at pages 34-38.
[2] *See* the Final Office Action at page 2.
[3] *See id.* at page 4.

claims is provided in the Claims Appendix.

STATUS OF AMENDMENTS
(37 C.F.R. § 41.37(c)(1)(iv))

The Applicants have not amended any claims subsequent to the final rejection of claims 1-33 by the Final Office Action.

SUMMARY OF CLAIMED SUBJECT MATTER
(37 C.F.R. § 41.37(c)(1)(v))

The invention of claim 1 is illustratively described in the Specification of the present application at, for example, paragraphs [17] and [18]. Certain embodiments of the present invention may found in a system and method for TCP offloading.[4] The system may comprise a host comprising a host memory and a network interface card (NIC) coupled to the host.[5] The NIC may comprise at least one TCP enabled Ethernet controller (TEEC).[6] The TEEC may comprise at least one internal elastic buffer.[7] In this regard, the TEEC may comprise a receive internal elastic buffer and/or a transmit internal elastic buffer.[8] The TEEC may be configured to process an incoming TCP packet once without any assembly.[9] In this regard, the TEEC may process an incoming TCP packet once without assembling the TCP packet data with the TCP data from adjacent packets for the same flow, and temporarily buffer at least a portion of the

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[4] *See* Application at page 7, lines 2-3.
[5] *See id.* at page 7, lines 3-4.
[6] *See id.* at page 7, lines 4-5.
[7] *See id.* at page 7, lines 5-6.
[8] *See id.* at page 7, lines 6-7.
[9] *See id.* at page 7, lines 7-8.

incoming TCP packet in the internal elastic buffer.[10] At least a portion of the incoming TCP packet may be temporarily buffered in the receive internal elastic register.[11] In a somewhat similar manner, at least a portion of a TCP packet that is to be transmitted may be temporarily buffered in the transmit internal elastic buffer.[12]

The TEEC may be adapted to place at least a portion of the incoming TCP packet data into at least a portion of the host memory.[13] The TEEC may place at least a data portion of an incoming TCP packet into a highest hierarchy of buffer available in the host memory by performing a single copy operation.[14] The TEEC may DMA transfer at least a portion of the processed incoming TCP packet to at least a portion of the host memory.[15] The TEEC may also place at least a portion of the processed incoming TCP packet into host buffers in the host memory for reassembly.[16] The TEEC may be a single chip, which may have at least one internal elastic buffer integrated therein.[17] In this regard, the receive internal elastic buffer and the transmitted internal elastic buffers are integrated with the TEEC.[18]

Claims 2-15 are dependent upon claim 1.

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[10] *See id.* at page 7, lines 8-11.
[11] *See id.* at page 7, lines 11-13.
[12] *See id.* at page 7, lines 13-14.
[13] *See id.* at page 7, lines 15-16.
[14] *See id.* at page 7, lines 16-18.
[15] *See id.* at page 7, lines 18-20.
[16] *See id.* at page 7, lines 20-21.
[17] *See id.* at page 7, lines 21-22.
[18] *See id.* at page 7, lines 22-24.

The invention of claim 16 is illustratively described in the Specification of the present application at, for example, paragraphs [19] and [20]. The method for offloading TCP processing may comprise receiving an incoming TCP packet at a TEEC and processing at least a portion of the incoming packet once by the TEEC without having to do any reassembly or retransmission by the TEEC.[19] At least a portion of the incoming TCP packet may be buffered in at least one internal elastic buffer of the TEEC.[20] The internal elastic buffer may comprise a receive internal elastic buffer and/or a transmit internal elastic buffer.[21] At least a portion of the incoming TCP packet may be buffered in the receive internal elastic buffer.[22] At least a portion of the processed incoming TCP packet may be placed in a portion of a host memory.[23] In this regard, at least a portion of the processed incoming TCP packet may be placed in a highest hierarchy of buffer available in a host memory by performing a single copy operation.[24] At least a portion of the processed incoming TCP packet may be DMA transferred to a portion of the host memory.[25] In accordance with an aspect of the invention, TCP packets that are temporarily buffered in the internal elastic buffer do not comprise packets for reassembly and packets for retransmission.[26] A portion of the processed incoming TCP packet may be placed in host buffers located in a host

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[19] *See id.* at page 7, lines 25-27.
[20] *See id.* at page 7, line 27 – page 8, line 1.
[21] *See id.* at page 8, lines 1-2
[22] *See id.* at page 8, lines 2-3.
[23] *See id.* at page 8, lines 3-4.
[24] *See id.* at page 8, lines 4-7.
[25] *See id.* at page 8, lines 7-8.

memory for processing by a host processor or CPU.[27] The TEEC may be a single chip having at least one internal elastic buffer.[28] Notwithstanding, the receive internal elastic buffer and the receive internal elastic buffer may be integrated with the chip.[29]

Claims 17-24 are dependent upon claim 16.

The invention of claim 25 is illustratively described in the Specification of the present application at, for example, paragraph [21]. Another embodiment of the invention may also provide a machine-readable storage, having stored thereon, a computer program having at least one code section for providing TCP offload.[30] The at least one code section may be executable by a machine for causing the machine to perform steps as described above for TCP offload.[31]

Claims 26-33 are dependent upon claim 25.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 1-5 and 7-33 remain rejected under 35 U.S.C. 102(e) as being anticipated by Boucher.[32] Claim 6 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher.[33]

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[26] *See id.* at page 8, lines 9-11.
[27] *See id.* at page 8, lines 11-13.
[28] *See id.* at page 8, line 13.
[29] *See id.* at page 8, lines 14-15.
[30] *See id.* at page 8, lines 16-18.
[31] *See id.* at page 8, lines 18-19.
[32] *See* the Final Office Action at page 2.
[33] *See id.*

ARGUMENT
(37 C.F.R. § 41.37(c)(1)(vii))

The Final Office Action rejects claims 1-5 and 7-33 as being anticipated by Boucher. The Final Office Action also rejects claim 6 as being unpatentable over Boucher. Boucher, however, does not describe, teach or suggest every recited limitation within these claims. Moreover, the Final Office Action fails to establish a prima facie case of anticipation because it does not specifically point to every limitation of the rejected claims of the present application in Boucher.

The burden of establishing a prima facie case of anticipation resides with the Patent and Trademark Office.[34] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[35] Further, the "identical invention must be shown in as complete detail as is contained in... the claim."[36]

I. Boucher Does Not Anticipate Claims 1-5 and 7-33

The Applicants first turn to the rejection of claims 1-5 and 7-33 as being anticipated by Boucher.

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[34] *See* In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) quoting In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967).
[35] *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[36] *Richaradson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed.

A. Boucher Does Not Teach or Suggest "Processing Occurring Without Reassembly"

1. Response to the Final Office Action

The Final Office Action responds to the Applicants' previous remarks regarding Boucher not teaching or suggesting "processing occurring without reassembly" as follows:

> Applicant is utilizing the term "reassembly" in the claim for reassembling TCP/IP packets which were fragmented (see specification, page 11, ¶ 39).

See the Final Office Action at page 6.

Claim 1, for example, recites, in part, the following:

> at least one internal elastic buffer, wherein **said TEEC processes an incoming TCP packet** once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, **said processing occurring without reassembly**.

See claim 1 (emphasis added). Thus, the relevant processing is that which is performed by the TEEC with respect to an incoming TCP packet. This processing which is performed by the TEEC with respect to an incoming TCP packet occurs without reassembly.

The Office Action seemingly imports portions of the specification into the claims. *See* the Final Office Action at page 5 ("Applicant is utilizing the term in the claim for reassembling TCP/IP packets which were fragmented (see specification, page 11, ¶ 39)"). The Applicants are perplexed that the Office Action imports language from the

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Cir. 1989).

specification into the claims, because such a practice runs afoul of patent examining procedure. *See, e.g.,* Manual of Patent Examining Procedure at § 2111.01(I) ("One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification."). "Though understanding the claim language may be aided by explanations contained in the written description, **it is important not to import into a claim limitations that are not part of the claim**." *See id.* (emphasis added, internal citation omitted). The language of claim 1 is clear and should stand on its own, without limitations from the specification being read into it.

The Final Office Action further states the following:

> The memory used in the ASIC is not for this purpose [i.e., reassembly], rather this is done in the host memory as can be seen in '173, Figures 23 and Figure 2, of Boucher.

See the Final Office Action at page 6. The Applicants respectfully disagree.

The Final Office Action cites "ASIC 400 disclosed in Figure 21 of app. No. 09/464,283, USPN 6,427,173 incorporated by reference" as a TEEC. *See* August 19, 2005 Office Action at pages 3-4. Boucher states that in "one specific embodiment, NI device 102 is the Intelligent Network Interface Card (NIC) of FIGS. 21 and 22 of U.S. patent application Ser. No. 09/464,283 [United States Patent No. 6,427,173 ("Boucher '173")] (the entire disclosure of Ser. No. 09/464,283 is incorporated... by reference). *See* Boucher at column 1, lines 22-25. Boucher '173 states that "INIC card 200 includes a Physical Layer Interface (PHY) chip 2100, ASIC chip 400 and Dynamic

Random Access Memory (DRAM) 460." *See* Boucher '173 at column 24, lines 60-63. As noted above, the DRAM 460 is separate and distinct from the ASIC chip 400.

The ASIC chip 400 in Boucher includes a sequencers block 2102 that includes a data synchronization buffer and a data assembly register.

> ASIC chip 400 includes a Media Access Control (MAC) unit 402, a sequencers block 2102, SRAM control 442, SRAM 440, DRAM control 450, a queue manager 2103, a processor 470, and a PCI bus interface unit 468.... Sequencers block 2102 includes a transmit sequencer 2104, **a receive sequencer 2105**, and configuration registers 2106.

Id. at column 24, line 67 to column 25, line 13. As shown above, the receive sequencer 2105 is part of the sequencers block 2102, which is, in turn, part of the ASIC chip 400. Therefore, the ASIC chip 400 includes the receive sequencer 2105.

The receiver sequencer 2105 in Boucher itself does, in fact, include much more than mere memory, as suggested by the Final Office Action ("The memory used in the ASIC is not for this purpose..."). As shown below, the receiver sequencer 2105, which is part of the ASIC chip, includes a data assembly register.

> FIG. 22 is a more detailed diagram of receive sequencer 2105. Receive sequencer 2105 includes a data synchronization buffer 2200, a packet synchronization sequencer 2201, a **data assembly register 2202**, ...[.]

Id. at column 25, lines 17-21 (emphasis added). Clearly, the data assembly register 2202 is used to assemble data at the receive sequencer 2105, which is part of the ASIC chip 400. Data is assembled within the ASIC chip 400 (which the Office Action assumes is a TEEC), by way of at least the data assembly register 2202. Thus,

Boucher does not teach or suggest "processing occurring [by a TEEC] **without reassembly**," as recited in the claims of the present application, because reassembly is occurring at the ASIC chip 400 by way of the data assembly register 2202. At least for this reason, the Applicants respectfully submit that Boucher does not anticipate the claims of the present application.

2. Response to the Advisory Office Action of December 29, 2005

Furthermore, in response to the Applicants' previous remarks regarding Boucher not teaching or suggesting processing occurring without reassembly, the advisory office action of December 29, 2005 ("the Advisory Office Action") states the following:

> Applicant is attributing the assembling of a packet with the reassembly of a fragmented TCP/IP packet stream. Applicant should be advised that the claim must be determined in light of the specification, however no limitation has been imported into the claim. Applicant will appreciate that any reasonable definition in the art of the term "reassembly" will constitute "act of regenerating a long message from several packets generated by segmentation". The assembly register is used to flow data one byte at a time. Applicant is utilizing the common term of reassembly in the specification for reassembling packets, which is clearly not done on the NIC, rather in the host memory as shown in Figure 2 of Boucher. If Applicant wishes to use the term reassembly as what is done in the assembly register, a rejection under 35 USC 112, first paragraph is not enabling this definition of the claim. Applicant enables processing without reassembly of segmented packets, not processing without clocking data bits into a register. By this rationale, the rejection is maintained.

See the Advisory Office Action at page 2. The Applicants are puzzled by the above response as the Advisory Office Action states that "no limitation has been

imported into the claim." However, the Advisory Office Action, similarly to the Final Office Action, is clearly importing a definition of the term "reassembly" (as used above in the Advisory Office Action, to mean "act of regenerating a long message from several packets generated by segmentation") when interpreting claim 1 of the present application. The Applicants respectfully traverse the use of the above definition of "reassembly" to interpret the limitations of claim 1. The Applicants submit that the language of claim 1 is clear and should stand on its own, without additional limitations being read into it.

In addition, the Applicants continue to maintain that Boucher discloses that data is assembled within the ASIC chip 400 by way of at least the data assembly register 2202. For example, even though the shift register 2217 within the data assembly register 2202 "is loaded serially a single byte at a time," data shifted into the register 2217 "is examined at the register outputs by protocol analyzer 2203 which verifies checksums, and generates "status" information 2223." *See* Boucher '173, col. 27, lines 12-14 and 32-25.

Furthermore, *the Advisory Office Action acknowledges the following*:

> [t]he **packet** received by the RX sequencer 2105 is temporarily stored in the data sync buffer 2200 before it can be **assembled in the data assembly register 2202.**

See the Advisory Office Action at page 2, 5th paragraph. Clearly, **the data assembly register 2202 reassembles data, as correctly acknowledged by the**

Advisory Office Action, so that the checksum and status information may be generated within the ASIC 400. Therefore, Boucher does not teach or suggest "processing occurring without reassembly," as recited by the claims of the present application.

B. Boucher Does Not Teach Or Suggest "A TEEC Including At Least One Internal Elastic Buffer, Wherein The TEEC Processes An Incoming TCP Packet Once And Temporarily Buffers At Least A Portion Of Said Incoming TCP Packet In Said Internal Elastic Buffer"

1. Response to the Final Office Action

In response to the Applicants' previous remarks regarding Boucher not teaching or suggesting a TEEC including at least one internal elastic buffer, wherein the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, the Final Office Action states the following:

> Applicant will see that data synchronization buffer 2200 is a buffer on the ASIC chip (by virtue of being in the receive sequencer) and is not a multi megabyte memory that is utilized for packet reordering, reassembly or retransmission (**it is merely there to store the packet as it is clocked into the receive sequencer**). By this rationale, the data synchronization buffer is equivalent to the claimed internal elastic buffer.

See the Final Office Action at page 6 (emphasis added). The Applicants respectfully submit, however, that the synchronization buffer 2200 is not "merely there to store the packet as it is clocked into the receive sequencer," as shown below.

While Boucher '173 states that the receive sequencer 2105 includes a "data synchronization buffer 2200" (*See id.* at column 25, lines 19-20), Boucher also states the following:

> Receiver sequencer 2105 uses **the buffers in DRAM 460 to store incoming network packet data** as well as status information for the packet.

Id. at column 26, lines 3-5 (emphasis added). Thus, Boucher clearly states that the DRAM 460, not the data synchronization buffer 2200, stores incoming network packet data.

As noted above, DRAM 460 is separate and distinct from the ASIC 400. The ASIC 400, however, does not include at least one internal elastic buffer, wherein the ASIC processes an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet in the internal elastic buffer. Instead, the receive sequencer 2105 uses the buffers in DRAM 460 to store incoming network packet data, as noted above. Further, the ASIC chip 400 of Boucher, which the Final Office Action assumes is the TEEC, does not "process an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet" in the data synchronization buffer 2200, which the Office Action assumes is the internal elastic buffer. Boucher does not teach, nor suggest, a TEEC including at least one internal elastic buffer, wherein the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, as recited, for example, in claim 1 of the present application.

2. Response to the Advisory Office Action

Furthermore, in response to the Applicants' previous remarks regarding Boucher not disclose or suggesting a TEEC including at least one internal elastic buffer, where the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet in the internal elastic buffer, the Advisory Office Action states the following:

> Applicant is correct in the recitation of passages of Boucher, however the claimed elastic buffer temporarily buffers the data (emphasis on temporarily), this denotes that the data will be moved eventually. In the case of Boucher, the synchronization buffer 2200 (read elastic buffer) temporarily buffers the data which eventually is moved to the DRAM. Applicant merely states that a portion of the packet is stored in the buffer, and does not specify what is stored. In the case of Boucher, the packet received by the RX sequencer 2105 is temporarily stored in the data sync buffer 2200 before it can be assembled in the data assembly register 2202. By this rationale the rejection is maintained.

See the Advisory Office Action at page 2. The Applicants submit that Boucher does not disclose or suggest that the buffer 2200 of Boucher '173 is an elastic buffer. Boucher discloses that buffer 2200 is a data synchronization buffer, but not elasticity buffer, as recited by the Applicants. *See* Boucher '173, col. 25, lines 17-27. Furthermore, the Applicants continue to maintain that Boucher does not disclose or suggesting a TEEC including at least one internal elastic buffer, where the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet in the internal elastic buffer, as recited by the Applicants in

the present application. Thus, at least for the reasons stated above, the Applicants respectfully submit that Boucher does not anticipate the claims of the present application.

Claims 16 and 25 are similar in many respects to claim 1. Therefore, the Applicants submit that claims 16 and 25 are also allowable over the references cited in the Final Office Action and the Advisory Office Action at least for the reasons stated above with regard to claim 1. Claims 2-5, 7-15, 17-24 and 26-33 are claims that depend from their respective independent claims 1, 16 and 25, and are allowable over the references cited in the Final Office Action and the Advisory Office Action at least for the same reasons as discussed above. The Applicants submit additional arguments with respect to the dependent claims, as set forth below.

C. Rejection of Claim 2 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said at least one internal elastic buffer comprises at least one of a receive internal elastic buffer and a transmit internal elastic buffer," as recited by the Applicants in claim 1. The Advisory Office Action argues that the data synchronization buffer 2200 is in fact the "internal elastic buffer" claimed by the Applicants. *See* the Advisory Office Action, page 2. However, the Final Office Action argues that "the internal elastic buffer comprises a receive internal elastic buffer 2105 and a transmit internal elastic buffer 2104." *See* the Final Office Action, page 3. The Applicants

submit that Boucher does not disclose or suggest an internal elastic buffer as claimed by the Applicants in claim 1, at least for the reasons stated above with regard to the rejection of claim 1. In addition, the Applicants would like to point out that the combination of arguments from the Advisory Office Action and the Final Office Action as relating to claim 2 are not factually correct since **the data synchronization buffer 2200 cannot comprise the receive internal elastic buffer 2105 and the transmit internal elastic buffer 2104**. Accordingly, the Applicants submit that claim 2 is allowable.

D. Rejection of Claims 3 and 4 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said at least a portion of said incoming TCP packet is temporarily buffered in said receive internal elastic buffer" and "at least a portion of a TCP packet to be transmitted is temporarily buffered in said transmit internal elastic buffer," as recited by the Applicants in claims 3 and 4. The Final Office Action refers for support to Boucher '173, col. 17, lines 35-67 and col. 25, lines 1-15. The Applicants submit that the cited portions of Boucher do not disclose or suggest the above limitations of claims 3 and 4. For example, Boucher '173 states the following:

> The SRAM and DMA controllers 444 interact across line 446 with external memory control 450 to send and receive frames via external memory bus 455 to and from dynamic random access memory (DRAM) buffers 460, which is located adjacent to the IC chip 400.

See Boucher '173, col. 17, lines 52-57. In this regard, Boucher discloses that the DRAM 460, not the data synchronization buffer 2200 or any of the buffers 2104 or 2105, stores incoming network packet data. Accordingly, the Applicants submit that claims 3 and 4 are allowable.

E. Rejection of Claim 5 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said TEEC places at least a portion of said incoming TCP packet data into at least a portion of a host memory," as recited by the Applicants in claim 5 of the present application. The Final Office Action refers for support to Figure 2 and col. 5, lines 50-55 of Boucher. The Applicants submit that the cited portions of Boucher do not disclose or suggest the above limitation of claim 5. For example, Boucher discloses that incoming packets are being processed on the NI device 102 (such as removal of TCP and IP headers) rather than being saved in a host memory. *See* Boucher, col. 5, lines 50-55. Furthermore, as stated above, incoming network packet data is stored by the DRAM 460 located within the INIC 200, and not in host memory. Accordingly, the Applicants submit that claim 5 is allowable.

F. Rejection of Claim 7 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the

limitation of "out-of-order TCP packets are not at least one of stored, re-ordered and re-assembled in a TEEC buffer," as recited by the Applicants in claim 7 of the present application. The Final Office Action refers for support to only Figure 2 of Boucher and states the following:

> Boucher discloses out of order TCP packets are not reordered in a TEEC buffer (i.e. they are reordered in the host memory).

See the Final Office Action, page 3. The Applicants traverse the Examiner's interpretation stated in parenthesis and submit that the limitations of claim 7 are clearly stated in claim 7 as is. The Applicants submit that Boucher, including Figure 2 of Boucher, does not disclose or suggest the above limitation of claim 7 with regard to processing of out-of-order TCP packets. Accordingly, the Applicants submit that claim 7 is allowable.

G. Rejection of Claim 8 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said NIC does not require a dedicated memory for re-ordering out-of-sequence TCP packets," as recited by the Applicants in claim 8 of the present application. The Final Office Action refers for support to only Figure 2 of Boucher and states the following:

> Boucher discloses said NIC does not require a dedicated memory for reordering out of sequence TCP packets (i.e. the host memory is used).

See the Final Office Action, page 3. The Applicants traverse the Examiner's interpretation stated in parenthesis and submit that the limitations of claim 8 are clearly stated in claim 8 as is. The Applicants submit that Boucher, including Figure 2 of Boucher, does not disclose or suggest the above limitation of claim 8 with regard to reordering out-of-sequence TCP packets. Accordingly, the Applicants submit that claim 8 is allowable.

H. Rejection of Claims 10-13 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said TEEC places at least data from said incoming TCP packet into a highest hierarchy of buffer available in a host memory by performing a single copy operation," as recited by the Applicants in claim 10 of the present application. The Final Office Action states the following:

> Claims 10-13 are rejected for similar reasons as stated above (i.e. the Office takes the term "highest hierarchy" as the best place to put the information, and "single copy operation" as a DMA transfer).

See the Final Office Action, page 3. The Applicants traverse the Examiner's interpretations stated in parenthesis and submit that the limitations of claims 10-13 are clearly stated in claim 10-13. The Applicants further traverse the Examiner's use of the definitions of "highest hierarchy" and "single copy operation," and submit that the

limitations of claims 10-13 are sufficiently clear. The Applicants submit that Boucher does not disclose or suggest the limitations of claims 10-13 and, therefore, claims 10-13 are allowable.

I. Rejection of Claim 14 under 35 U.S.C. § 102(e)

The Applicants submit that Boucher does not disclose or suggest at least the limitation of "said TEEC comprises a single chip, having integrated therein, said at least one internal elastic buffer," as recited by the Applicants in claim 14 of the present application. The Final Office Action states the following:

> Boucher discloses the TEEC comprises a single chip having the buffer integrated therein (i.e. integrated into the Apollo VT 8501 MVP4 Northridge chip).

See the Final Office Action, page 4. The Applicants submit that Boucher does not disclose or suggest the above limitation of claim 14 with regard to the integration of the internal elastic buffer within a single chip TEEC, at least for the reasons stated above with regard to allowability of claim 1. More specifically, Boucher does not disclose or suggest an internal elastic buffer as recited by the Applicants in claim 1. Accordingly, the Applicants submit that claim 14 is allowable.

II. Inherency

With respect to claim 9, the August 19, 2005 Office Action asserted that "it is inherent that any packet received would be inserted in its correct placement in host

memory as shown by Figure 2." *See* August 19, 2005 Office Action at page 5. The Applicants previously submitted that absent a "basis in fact and/or technical reasoning" for the rejection of record, that rejection should be reconsidered and withdrawn. *See* September 15, 2005 Amendment at pages 14-16. In response, the Final Office Action states the following:

> Applicant is invited to look at Figure 2 of Boucher, where it is shown that subsequent data packets are received onto the NI device, which have headers stripped, and then the data is DMA'd directly over to the host memory, no reassembly is done in the NIC device, the reassembly is done at the host memory. By this rationale, the rejection is maintained.

See October 7, 2005 Office Action at page 6.

Initially, the Applicants respectfully submit and reiterate that the ASIC 400 of Boucher performs reassembly, as shown and detailed above. Also, claim 9 recites, in part, "said NIC does not require a dedicated memory for assembling and re-ordering IP packets fragmented at the IP layer." The August 19, 2005 Office Action affirmatively recited that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2."

The Applicants respectfully disagree with this statement of inherency. For example, when a packet is received in error it must be retransmitted. As a result, packets are often received out-of-order. If the out-of-order packets are to be assembled by the NIC and sent up to the host, a larger ON-NIC memory is required to store and reassemble the out-of-order packets. After the packets are reassembled on the NIC, the packets are posted in the host buffer, and the host is informed that the

buffer is posted. The Applicants note that claim 1, for example, recites an "elastic buffer," not a dedicated ON-NIC memory. The Applicants respectfully maintain that it is **not** inherent that any packet received would be inserted in its correct placement in the host memory.

The Applicants once again reviewed and analyzed Figure 2 of Boucher, and maintain that there is nothing in that Figure to lead one to conclude that any packet that is received would **necessarily** be inserted in its correct placement in host memory, as asserted by the Final Office Action.

Additionally, claim 9 recites that the "NIC," not the host, "does not require a dedicated memory for assembling and reordering IP packets fragmented at the IP layer." The Office Action, however, concludes that Figure 2 shows placement in the host memory.

The Applicants submit that a rejection based on inherency **must** include a statement of the rationale or evidence tending to show inherency. *See* Manual of Patent Examining Procedure at § 2112. "The fact that a certain result or characteristic **may** occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *See id. citing In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result

from a given set of circumstances is not sufficient.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The Applicants respectfully submit that neither Boucher itself nor the Final Office Action "make[s] clear that the missing descriptive matter," said to be inherent, i.e., that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2," is "**necessarily present** in" Boucher.

A rejection based on inherency must be based on factual or technical reasoning:

> In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teaching of the applied prior art.

Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

The Applicants respectfully submit that the Final Office Action does not contain a basis in fact and/or technical reasoning to support the rejection based on inherency. Instead, as recited above, at least claim 9 of the present application stands rejected based on a conclusory statement of inherency, rather than upon a "basis in fact and/or technical reasoning." Accordingly, the Applicants respectfully maintain that, absent a "basis in fact and/or technical reasoning" that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2" with respect to the rejection of claim 9, that rejection should be reconsidered and withdrawn.

III. Boucher Does Not Render Claim 6 Unpatentable

Claim 6 stands rejected under 35 USC 103(a) as being unpatentable over Boucher. Initially, MPEP 2142 states that in order for a prima facie case of obviousness to be established, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations**. Further, MPEP 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination," and that "although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so'" (citing In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)). Moreover, MPEP 2143.01 also states that the level of ordinary skill in the art cannot be relied upon to provide the suggestion...," citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999). Therefore, since claim 6 is dependent on claim 1, the Applicants respectfully submit that claim 6 should be in condition for allowance, at least for the reasons set forth above with respect to claim 1.

Additionally, however, Applicants submit that claim 6 is allowable for the following additional reasons. Specifically, claim 6 recites that the "NIC utilizes only said

at least one internal elastic buffer to temporarily buffer said at least a portion of said incoming TCP packet." The August 19, 2005 Office Action states the following:

> Boucher does not specifically state that only the elastic buffer is used to temporarily buffer at least a portion of the incoming TCP packet, however, it is well known that elastic buffers are used to buffer packets (i.e., receiving FIFO's for routers, etc.). By this rationale, **"Official Notice"** is taken that both the concept and advantages of providing for utilizing only the elastic buffer to temporarily buffer a portion of the TCP packet is well known and expected in the art.

See August 19, 2005 Office Action at page 6 (emphasis added). Further, the Final Office Action maintains that "Boucher does not specifically state that **only** the elastic buffer is used to temporarily buffer at least a portion of the incoming TCP packet." *See* October 7, 2005 Office Action at pages 4-5.

The Applicants traversed the clear assertion of Official Notice that "both the concept and advantages of providing for utilizing only the elastic buffer to temporarily buffer a portion of the TCP packet is well known and expected in the art." *See,* September 15, 2005 Amendment at pages 16-18. In response, the Final Office Action states the following:

> [T]he Office provides Susnow et al (USPN 6,751,235) as support that only the elastic buffer is used to temporarily buffer at least a portion of the incoming packet. As shown in Figure 8, and col., 7, lines 30-55. It can clearly be seen that the elastic buffer is used to transition data from a network link to the core clock domain of the VXB (i.e. virtual expansion bridge) thereby removing the chance of providing data overflow or underflow. By this rationale, the Office has satisfied its burden of proof that an elastic buffer can be

> used to buffer a portion of an incoming packet is well known in the art.

See October 7, 2005 Office Action at pages 6-7. In short, the present Office Action asserts that it has satisfied it burden of proof "that an elastic buffer can be used to buffer a portion of an incoming packet."

In addition, the Advisory Office Action states the following:

> Susnow discloses that the data is temporarily stored **only** by the elastic buffer. The data is temporarily buffered in the elastic buffer in order to transition from a network link into the core clock domain without data overflow or underflow. Applicant is advised to consult the teaching of any common computer networking reference to understand the benefits of data underflow or overflow, as the elastic buffer temporarily buffers the data into the system. Applicant has clearly not shown why the reference of Susnow does not disclose the limitation of claim 6 and the Office reaffirm that the burden of proof has been met by the Examiner. BY [sic] this rational the rejection is maintained.

See the Advisory Office Action, page 2 (emphasis added). The Applicants submit that Susnow **does not disclose or suggest** that "data is temporarily stored **only** by the elastic buffer," as claimed by the Advisory Office Action.

The Final Office Action, however, rejects claim 6 of the present application through an assertion of Official Notice. Claim 6 recites the following:

> The system according to claim 1, wherein said NIC utilizes **only said at least one internal elastic buffer** to temporarily buffer said at least a portion of said incoming TCP packet.

The Applicants are not disputing that elastic buffers exist. Further, United States Patent No. 6,751,235 ("Susnow") does, indeed, disclose an elastic buffer. *See* Susnow at column 7, lines 35-39 ("FIG. 8 illustrates an example block diagram of Elastic Buffer 682 provided to transition data from a network link into the core clock domain of VXB 670 responsible for transferring that data to MCH 620 without data overflow or data underflow....").

Claim 6, however, recites that "**only** said at least one **internal** elastic buffer [is utilized] to temporarily buffer said at least a portion of said incoming TCP packet." Further, even assuming the Final Office Action has "satisfied its burden of proof that an elastic buffer can be used to buffer a portion of an incoming packet," the Final Office Action still does not show a reference in which "**only** said at least one internal elastic buffer is utilized to temporarily buffer said at least a portion of said incoming TCP packet." Thus, the Applicants reaffirm the traversal of Official Notice. Under MPEP 2144.03, the Examiner continues to be obligated to provide a reference(s) in support of the assertion of Official Notice with respect to claim 6 (i.e., "**only** said at least one internal elastic buffer [is utilized] to temporarily buffer said at least a portion of said incoming TCP packet") if the Examiner intends to maintain any rejection based on the assertion of Official Notice. Additionally, the Applicants respectfully request the Examiner reconsider the assertion of Official Notice and provide to Applicants any basis for the assertion of Official Notice.

IV. Rejection of Claims 2-15, 17-24, and 26-33

Based on at least the foregoing, the Applicants believe the rejection of independent claims 1, 16, and 25 under 35 U.S.C. § 102(e) as being anticipated by Boucher has been overcome and request that the rejection be withdrawn. Additionally, claims 2-15, 17-24, and 26-33 depend from independent claims 1, 16, and 25, respectively, and are, consequently, also respectfully submitted to be allowable.

CONCLUSION

For at least the foregoing reasons, the Applicants submit that claims 1-5 and 7-33 are not anticipated by Boucher. Furthermore, the Applicants submit that claim 6 is not unpatentable over Boucher. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge $500 (to cover the Brief on Appeal Fee) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: 15-MAY-2006

By: _____
Ognyan Beremski, Reg. No. 51,458
Attorney for Applicants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775 – 8100

CLAIMS APPENDIX
(37 C.F.R. § 41.37(c)(1)(viii))

1. A system for offloading TCP processing, the system comprising:

a host;

a network interface card (NIC) coupled to said host, said NIC comprising,

a TCP enabled Ethernet controller (TEEC), said TEEC comprising,

at least one internal elastic buffer, wherein said TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, said processing occurring without reassembly.

2. The system according to claim 1, wherein said at least one internal elastic buffer comprises at least one of a receive internal elastic buffer and a transmit internal elastic buffer.

3. The system according to claim 2, wherein said at least a portion of said incoming TCP packet is temporarily buffered in said receive internal elastic buffer.

4. The system according to claim 2, wherein at least a portion of a TCP packet to be transmitted is temporarily buffered in said transmit internal elastic buffer.

5. The system according to claim 1, wherein said TEEC places at least a portion of said incoming TCP packet data into at least a portion of a host memory.

6. The system according to claim 1, wherein said NIC utilizes only said at least one internal elastic buffer to temporarily buffer said at least a portion of said incoming TCP packet.

7. The system according to claim 1, wherein out-of-order TCP packets are not at least one of stored, re-ordered and re-assembled in a TEEC buffer.

8. The system according to claim 1, wherein said NIC does not require a dedicated memory for re-ordering out-of-sequence TCP packets.

9. The system according to claim 1, wherein said NIC does not require a dedicated memory for assembling and re-ordering IP packets fragmented at the IP layer.

10. The system according to claim 1, wherein said TEEC places at least data

from said incoming TCP packet into a highest hierarchy of buffer available in a host memory by performing a single copy operation.

11. The system according to claim 1, wherein said TEEC DMA transfers at least a portion of said processed incoming TCP packet to at least a portion of a host memory.

12. The system according to claim 1, wherein said NIC does not require a TCP offload engine (TOE) dedicated memory for at least one of packet retransmission and packet reassembly.

13. The system according to claim 1, wherein said TEEC places at least a portion of said processed incoming TCP packets into host buffers in a host memory for reassembly.

14. The system according to claim 1, wherein said TEEC comprises a single chip, having integrated therein, said at least one internal elastic buffer.

15. The system according to claim 1, wherein said TEEC comprises a single

chip, having integrated therein, said at least one internal elastic buffer, and no internal buffers and interfaces to external buffers, that are utilized for at least one of packet retransmission, packet reassembly and packet re-ordering.

16. A method for offloading TCP processing, the method comprising:

receiving an incoming TCP packet at a TCP enabled Ethernet controller (TEEC);

processing at least a portion of said incoming packet once by said TEEC without reassembly; and

temporarily buffering said at least a portion of said incoming TCP packet in at least one internal elastic buffer of said TEEC.

17. The method according to claim 16, wherein said at least one internal elastic buffer comprises at least one of a receive internal elastic buffer and a transmit internal elastic buffer.

18. The method according to claim 17, further comprising temporarily buffering said at least a portion of said incoming TCP packet in said receive internal elastic buffer.

19. The method according to claim 16, further comprising placing at least a portion of said processed at least a portion of said incoming packet in at least a portion of a host memory.

20. The method according to claim 16, wherein said placing further comprises placing at least a portion of said processed incoming TCP packet in a highest hierarchy of buffer available in a host memory by performing a single copy operation.

21. The method according to claim 16, further comprising DMA transferring at least a portion of said processed incoming TCP packet in at least a portion of a host memory.

22. The method according to claim 16, wherein packets temporarily buffered in said in at least one internal elastic buffer are not buffered for at least one of reassembly and retransmission.

23. The method according to claim 16, further comprising placing at least a portion of said processed incoming TCP packet in host buffers in a host memory for processing.

24. The method according to claim 16, wherein said TEEC comprises a single chip, having integrated therein, said at least one internal elastic buffer.

25. A machine-readable storage, having stored thereon, a computer program having at least one code section for providing TCP offload, the at least one code section being executable by a machine for causing the machine to perform steps comprising:

receiving an incoming TCP packet at a TCP enabled Ethernet controller (TEEC);

processing at least a portion of said incoming packet once by said TEEC without reassembly; and

temporarily buffering said at least a portion of said incoming TCP packet in at least one internal elastic buffer of said TEEC.

26. The machine-readable storage according to claim 25, wherein said at least one internal elastic buffer comprises at least one of a receive internal elastic buffer and a transmit internal elastic buffer.

27. The machine-readable storage according to claim 26, code for temporarily buffering said at least a portion of said incoming TCP packet in said receive internal elastic buffer.

28. The machine-readable storage according to claim 25, further comprising code for placing at least a portion of said processed at least a portion of said incoming packet in at least a portion of a host memory.

29. The machine-readable storage according to claim 25, further comprising code for placing at least a portion of said processed incoming TCP packet in a highest hierarchy of buffer available in a host memory by performing a single copy operation.

30. The machine-readable storage according to claim 25, further comprising code for DMA transferring at least a portion of said processed incoming TCP packet in at least a portion of a host memory.

31. The machine-readable storage according to claim 25, wherein packets temporarily buffered in said in at least one internal elastic buffer are not buffered for at least one of reassembly and retransmission.

32. The machine-readable storage according to claim 25, further comprising code for placing at least a portion of said processed incoming TCP packet in host buffers in a host memory for processing.

33. The machine-readable storage according to claim 25, wherein said TEEC comprises a single chip, having integrated therein, said at least one internal elastic buffer.

EVIDENCE APPENDIX
(37 C.F.R. § 41.37(c)(1)(ix))

(1) United States Patent No. 6,757,746 ("Boucher"), entered into record by the Examiner in the August 19, 2005 Office Action.

(2) United States Patent No. 6,427,173 ("Boucher '173"), entered into record by the Examiner in the August 19, 2005 Office Action.

(3) United States Patent No. 6,751,235 ("Susnow"), entered into record by the Examiner in the October 7, 2005 Office Action.

RELATED PROCEEDINGS APPENDIX
(37 C.F.R. § 41.37(c)(1)(x))

Not applicable.